ABSTRACT

A semiconductor memory device comprises: an etch stop layer formed on an interconnect stack; a contact stud penetrating the etch stop layer and provided in the interconnect stack of a memory cell to make electrical connection to a diffusion layer of the memory cell transistor; a contact stud penetrating the etch stop layer and provided in the interconnect stack of a plate transistor to make electrical connection to a diffusion layer of the plate transistor; a ferro-electric capacitor formed on the contact stud of the memory cell transistor; an interlayer insulation film formed to cover an upper electrode of the ferro-electric capacitor and the contact stud of the plate transistor; and a plate line providing an electrical connection between the upper electrode of the ferro-electric capacitor and the contact stud of the plate transistor through contact holes formed in the interlayer insulation film.